In the Claims

Claims 1-20 and 31-50 are canceled.

Cancel claims 51-60.

21. [Original] A semiconductor processing method comprising forming two series of field effect transistors over a substrate, one series being isolated from adjacent devices by shallow trench isolation, the other series having active area widths greater than one micron, the one series being formed to have active area widths less than one micron to achieve lower threshold voltages than the other of the series.

22. [Original] The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by a common channel implant.

23. [Original] The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by a common channel implant, said implant being the only channel implant which defines the threshold voltages for the two series of field effect transistors.

24. [Original] The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants.

25. [Original] The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants, said common channel implants being the only channel implants which define the threshold voltages for the two series of field effect transistors.

26. [Original] A semiconductor processing method comprising forming two series of field effect transistors over a substrate, at least one series being isolated from adjacent devices by shallow trench isolation, and further comprising achieving different threshold voltages between field effect transistors in different series by varying the active area widths of the field effect transistors in the series, at least one series having active area widths less than one micron.

27. [Original] The semiconductor processing method of claim 26, wherein the threshold voltages for the two series of field effect transistors are defined by a common channel implant.

28. [Original] The semiconductor processing method of claim 26, wherein the threshold voltages for the two series of field effect transistors are defined by a common channel implant, said implant being the only channel implant which defines the threshold voltages for the two series of field effect transistors.

29. [Original] The semiconductor processing method of claim 26, wherein the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants.

30. [Original] The semiconductor processing method of claim 26, wherein the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants, said common channel implants being the only channel implants which define the threshold voltages for the two series of field effect transistors.

61. [New] The semiconductor processing method of claim 21, wherein the transistors of the two series comprise transistors having a single geometry type.

62. [New] The semiconductor processing method of claim 61, wherein the transistors of the single geometry type comprise planar transistors.

63. [New] The semiconductor processing method of claim 21, further comprising performing a common channel implant within active areas of the transistors of the two series at the same moment in time.

64. [New] The semiconductor processing method of claim 21, further comprising performing a common channel implant within active areas of both of the series of the transistors at the same moment in time to define the different threshold voltages of the transistors of the two series.

65. [New] The semiconductor processing method of claim 64, wherein the common channel implant is the only channel implant which defines the different threshold voltages of the transistors of the two series.

66. [New] The semiconductor processing method of claim 21, further comprising implanting an impurity into active areas of the transistors of the two series at the same moment in time.

67. [New] The semiconductor processing method of claim 21, further comprising implanting an impurity into active areas of the transistors of the two series at the same moment in time to simultaneously define the different threshold voltages of the transistors of the two series.

68. [New] The semiconductor processing method of claim 67, wherein the implanting of the impurity is the only implant which defines the different threshold voltages of the transistors of the two series.

69. New] The semiconductor processing method of claim 22, wherein the common channel implant comprises implanting a single type of impurity.

70. [New] The semiconductor processing method of claim 22, wherein the common channel implant comprises implanting a single type of impurity to define the different voltage thresholds of the transistors of the two series.

71. [New] The semiconductor processing method of claim 26, wherein the transistors of the two series comprise transistors having a single geometry type.

72. [New] The semiconductor processing method of claim 71, wherein the transistors of the single geometry type comprise planar transistors.

73. [New] The semiconductor processing method of claim 26, further comprising performing a common channel implant within active areas of the transistors of the two series at the same moment in time.

74. [New] The semiconductor processing method of claim 26, further comprising performing a common channel implant within active areas of both of the series of the transistors at the same moment in time to define the different threshold voltages of the transistors of the two series.

75. [New] The semiconductor processing method of claim 74, wherein the common channel implant is the only channel implant which defines the different threshold voltages of the transistors of the two series.

76. [New] The semiconductor processing method of claim 26, further comprising implanting an impurity into active areas of the transistors of the two series at the same moment in time.

77. [New] The semiconductor processing method of claim 26, further comprising implanting an impurity into active areas of the transistors of the two series at the same moment in time to simultaneously define the different threshold voltages of the transistors of the two series.

78. [New] The semiconductor processing method of claim 77, wherein the implanting of the impurity is the only implant which defines the different threshold voltages of the transistors of the two series.

79. [New] The semiconductor processing method of claim 27, wherein the common channel implant comprises implanting a single type of impurity.

80. [New] The semiconductor processing method of claim 27, wherein the common channel implant comprises implanting a single type of impurity to define the different voltage thresholds of the transistors of the two series.